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EE 220

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Lab 06: Oscilloscope/Logic Analyzer

**Toggle circuit Verilog code**

// A D flip flop

module FF\_DC(q, clk, clr, d);

input clk, clr, d;

output reg q;

always @(posedge clk)

if(clr)q<=0;

else q<=d;

endmodule

// Toggle circuit

module toggle(q\_out, clk\_out, g\_clk, clr);

input g\_clk;

input clr;

output q\_out;

output clk\_out;

wire q\_not;

// read from the output, huh

not(q\_not, q\_out);

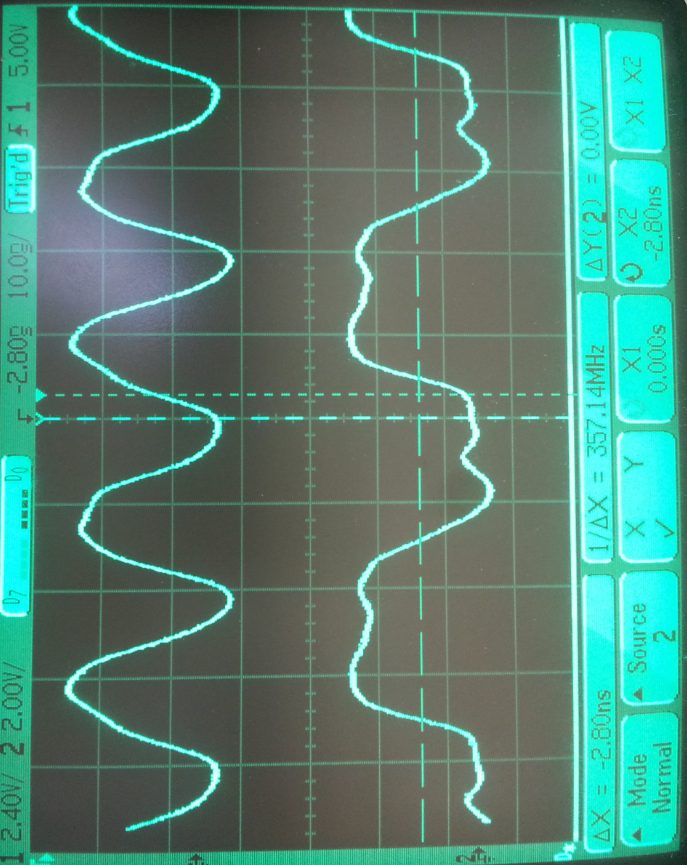
// Not quite sure how buf works

buf(clk\_out, g\_clk);

FF\_DC flip(q\_out, g\_clk, clr, q\_not);

endmodule

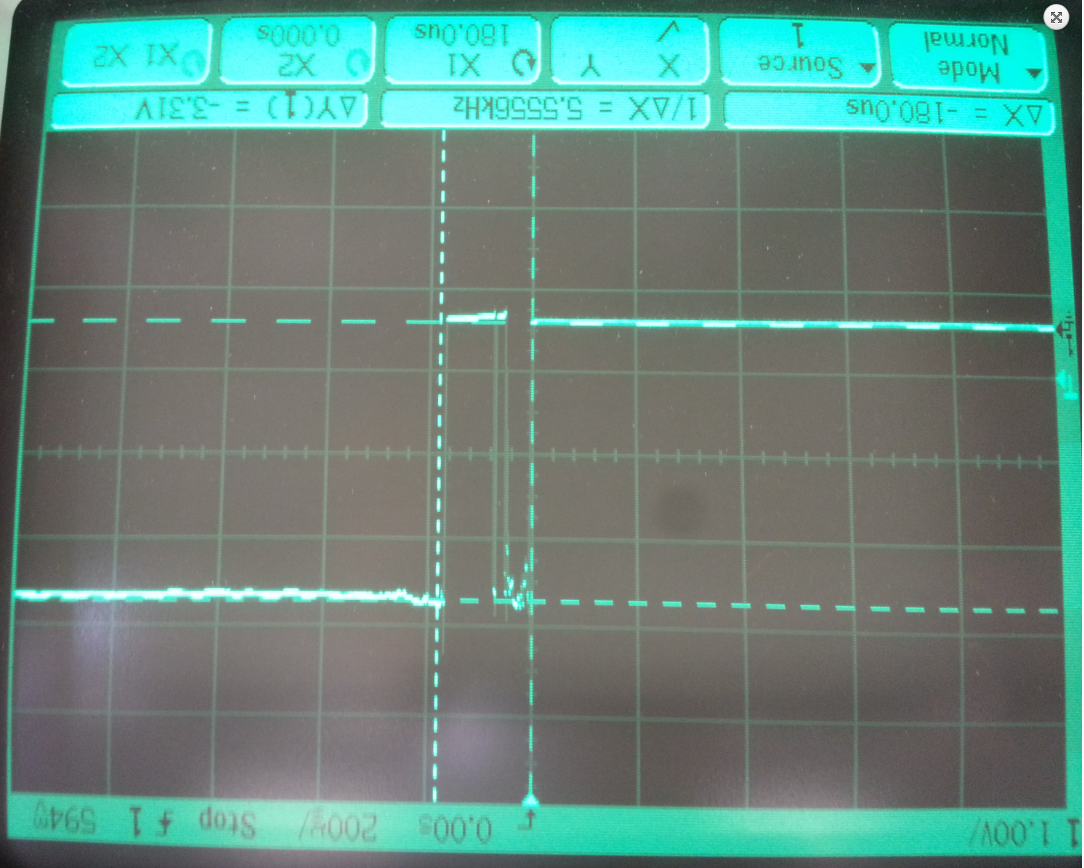
**Toggle Circuit screen capture**



**Toggle circuit question and answer- Why are the waves not square?**

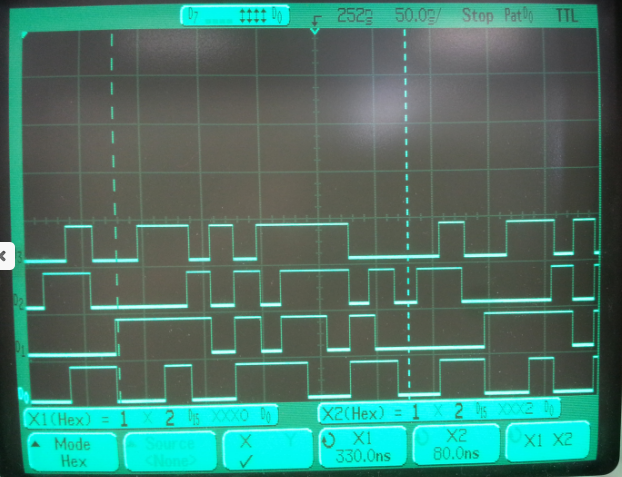
Because outputting perfect square waves is not only impossible, it is useless for a digital device like the FPGA we are using. When we put cutoffs on the wave, and consider everything higher than the cutoff to be ‘1’ and everything lower to be a ‘0’, then we get our nice digital toggle signal. The end.

**Bounce screen capture**



**Bounce circuit settling time: 180 us**

**4-bit shifter screen capture**



**4-bit shifter pattern of values**

***04D12AB6879FEC35***

**Anomalies**

The first breadboard I tried to do the bounce circuit on didn’t have any power going to VCC. So I had to change that. Also, when connecting up the wires for the 4-bit shifter, I initially could not get any signal on D3. But I got it.